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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,848	04/12/2004	Kazuhiko Miyata	0756-7278	2083

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EXAMINER	
TRAN, CON P	

ART UNIT	PAPER NUMBER
2614	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/821,848	MIYATA ET AL.	
	Examiner	Art Unit	
	CON P. TRAN	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-14 and 22-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-14 and 22-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/31/08 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 8-14, and 22-35** are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art Background of the Invention, Figures 2, 3, 4, 5 (hereinafter, "APA") in view of Nakagawa, et al. (hereinafter, "Nakagawa") U.S. Patent 5,650,834.

Regarding **claim 8**, APA teaches an audio signal processing circuit (307, Fig. 3) comprising: flexible circuit board (308, Fig. 3) and a chip capacitor mounted over (PCB 311, Fig. 3); and an equivalent circuit diagram showing a conventional audio signal processing circuit (401, Fig. 4) includes an operational amplifier (402, Fig. 4); external resistors (403, 404, 405, Fig. 4), external capacitors (406, 407, Fig. 4; see APA page 5, line 12 – page 6, line 12); wherein one terminal of resistor (404, Fig. 4) is connected to the operational amplifier (402, Fig. 4) and the other terminal of the resistor (404, Fig. 4) is connected to a capacitor (407, Fig. 4); flexible printed circuit (205, 305, Figs. 2B, 3B, APA, page 3, lines 7-8, lines 20-22) connected to substrate (see Figs. 2A, 2B, 3A, 3B); chip capacitor on flexible printed circuit (APA, page 3, lines 9-13).

APA does not explicitly disclose: a thin film element formed over an insulating substrate; a thin film resistor formed over the insulating substrate; and a chip capacitor mounted over a flexible printed circuit connected to the insulating substrate; and wherein one terminal of the thin film resistor is connected to the thin film element and the other terminal of the thin film resistor is connected to the chip capacitor.

Nakagawa discloses active-matrix substrate for use in matrix-type display devices such as liquid crystal display devices (col. 1, lines 7-10) including (see Figs. 1, 5A, 5B) thin film transistors arranged in a matrix pattern on the transparent insulative substrate (8, Fig. 5), a plurality of gate lines (11, Fig. 5) each adapted to supply a signal to a gate electrode of each of the thin film transistors (6, Fig. 5), and a thin film resistor

provided intermediate between an input terminal of each of the signal lines and shortcircuiting ring; capacitor (3, Fig. 1; see col. 4, lines 33-53; col. 6, lines 38-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporated the active-matrix substrates taught by Nakagawa with the audio signal processing circuit of APA to obtain the audio signal processing circuit claimed limitations since the claimed invention is merely a combination of old elements, and in the combination each element merely would have performed the same function as it did separately. The motivation is for purpose of improvements in production yield and product quality, as suggested by Nakagawa in column 3, lines 24-26.

Regarding **claim 9**, APA in view of Nakagawa teaches the audio signal processing circuit according to claim 8, wherein the audio signal processing circuit comprises an input circuit (see APA, page 6, line 25 – page 7 , line 4) and the input circuit comprises the thin film resistor (TFT 6, see Nakagawa, Fig. 5) and the chip capacitor (APA, page 5, lines 13-16).

Regarding **claim 10**, APA in view of Nakagawa teaches the audio signal processing circuit according to claim 8, wherein the audio signal processing circuit comprises a feedback circuit and the feedback circuit (feedback of amp. 402, see APA, Fig. 4) comprises the thin film resistor (TFT 6, see Nakagawa, Fig. 5) and the chip capacitor (APA, page 5, lines 13-16).

Regarding **claim 11**, APA in view of Nakagawa teaches the audio signal processing circuit according to claim 8, wherein the audio signal processing circuit comprises a smoothing circuit and the smoothing circuit comprises the thin film resistor (TFT 6, see Nakagawa, Fig. 5) and the chip capacitor the chip capacitor (APA, page 5, lines 13-16).

Regarding **claim 12**, APA in view of Nakagawa teaches the audio signal processing circuit according to claim 8, wherein P-type impurities are doped in the thin film resistor (contact holes 34, 35, see Nakagawa, Figs. 5a, 5b; col. 9, lines 5-10).

Regarding **claim 13**, APA in view of Nakagawa teaches the audio signal processing circuit according to claim 8, wherein the thin film resistor has a resistance value of 80 kΩ or more (APA, page 5, lines 19-21).

Regarding **claim 14**, APA in view of Nakagawa teaches electronic equipment comprising the audio signal processing circuit according to claim 8, wherein the electronic equipment is one selected from the group consisting of a video camera, a digital camera, a head mounted display, a game machine, a car navigation system, a personal computer and a portable information terminal (APA, page 1, line 13 – page 2 line 4; Nakagawa, col. 1, lines 17-29).

Regarding **claim 22,** this claim has similar limitations as Claim 8. Therefore it is interpreted and rejected under APA in view Nakagawa of for the reasons set forth in the rejection of Claim 1. It is noted the APA further discloses in Fig. 3 the display device has a substrate (309) on which a pixel portion (304, see Fig. 3, Specification page 3, lines 17-18); chip capacitor mounted around the pixel portion (i.e., chip capacitor on a substrate of a display device, see APA page 4, lines 13-18).

Regarding **claims 23-28,** these claims have similar limitations as Claims 9-14. Therefore they are interpreted and rejected under APA in view Nakagawa for the reasons set forth in the rejection of Claims 9-14.

Regarding **claim 29,** this claim has similar limitations as Claim 8. Therefore it is interpreted and rejected under APA in view Nakagawa of for the reasons set forth in the rejection of Claim 8. It is noted the APA further discloses in Fig. 3 the display device has a substrate (309) on which a pixel portion (304, see Fig. 3, Specification page 3, lines 17-18).

Regarding **claims 30-35,** these claims have similar limitations as Claims 9-14. Therefore they are interpreted and rejected under APA in view Nakagawa for the reasons set forth in the rejection of Claims 9-14.

Response to Arguments

4. Applicants' arguments with respect to claims 8-14 and 22-35 have been considered but are moot in view of the new grounds of rejection.

Regarding Applicants' arguments that APA and Nakagawa, alone or in combination, fail to disclose a chip capacitor mounted over a flexible printed circuit connected to an insulating substrate, examiner respectfully disagrees. As presented above in the Office Action, APA further discloses flexible printed circuit (205, 305, Figs. 2B, 3B, APA, page 3, lines 7-8, lines 20-22) connected to substrate (see Figs. 2A, 2B, 3A, 3B); chip capacitor on flexible printed circuit (APA, page 3, lines 9-13); and Nakagawa specifies the substrate being insulative substrate (8, see Fig. 5),

Regarding Applicants' arguments that APA and Nakagawa, alone or in combination, fail to disclose a chip capacitor mounted around the pixel portion and over the insulating substrate, examiner respectfully disagrees. As presented above in the Office Action, APA further discloses in Fig. 3 the display device has a substrate (309) on which a pixel portion (304, see Fig. 3, Specification page 3, lines 17-18); chip capacitor mounted around the pixel portion (i.e., chip capacitor on a substrate of a display device, see APA page 4, lines 13-18).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CON P. TRAN whose telephone number is (571)272-7532. The examiner can normally be reached on M - F (08:30 AM - 05:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor VIVIAN C. CHIN can be reached on 571-272-7848. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/CPT/
March 19, 2009

/Vivian Chin/

Supervisory Patent Examiner, Art Unit 2614